CLAIMS

1. A method for reducing switching activity during a test scan operation of at least one scan chain in an integrated circuit (IC) comprising the steps of:

a) determining stimulus and result value probabilities for a plurality of memory elements in said IC; and

b) connecting said memory elements to form at least one scan chain based on said probabilities, thereby reducing the switching activity as determined by the probabilities and by the ordering of said memory elements within said at least one scan chain.

2. The method of claim 1, wherein said stimulus and result probabilities are determined by generating and simulating a set of test patterns for said IC.

3. The method of claim 1, wherein each of said stimulus and result value probabilities comprise the probability that the stimulus value for a selected memory element coincides with the result value for said selected memory element.

4. The method of claim 1, wherein each of said stimulus and result value probabilities comprise a probability that the stimulus value for a selected memory element is the opposite of the result value for said selected memory element.

5. The method of claim 1, wherein said stimulus and result probabilities comprise for at least one pair of memory elements whose first element has a stimulus value s1 and a result value r1 and whose second element has a stimulus value s2 and a result value r2, the probability that the stimulus value s1 equals s2 and the probability that the result value r1 equals r2.

6. The method of claim 5, wherein the probability that said at least one pair of memory elements will be connected sequentially in at least one of said scan chain increases with a probability that the stimulus value s1 equals s2 and the result value r1 equals r2, said probability being computed from said probability that the stimulus value s1 equals s2 and said probability that the result value r1 equals r2.

7. The method of claim 5, wherein the probability that said at least one pair of memory elements will be connected sequentially in said at least one scan chain increases with a probability that the stimulus value s1 differs from s2 and the result value r1 differs from r2, said probability being computed from said probability that the stimulus value s1 equals s2 and said probability that the result value r1 equals r2.

8. The method of claim 3, wherein the probability that at least one pair of said memory elements will be connected sequentially in said at least one scan chain increases with a probability that the stimulus and the result values coincide for both elements of said pair, said probability of stimulus and result values coinciding for both elements of said pair being computed from said probabilities that the stimulus and result values for each of said memory elements coincide.

9. The method of claim 4, wherein the probability that at least one pair of said memory elements will be connected sequentially in said at least one scan chains increases with a probability that the stimulus and the result values are opposite for both elements of said pair, said probability of stimulus and result values being opposite for both elements of said pair being computed from said probabilities that the stimulus and result values for each of said memory elements are opposite.

10. The method of claim 5, wherein the probability that at least one pair of said memory elements will be connected sequentially in at least one of said scan chains decreases with a probability that the stimulus value s1 does not equal s2 and the result value r1 equals r2, said probability being computed from said probability that the stimulus value s1 equals s2 and said probability that the result value r1 equals r2.

11. The method of claim 5, wherein the probability that at least one pair of said memory elements will be connected sequentially in at least one of said scan chains decreases with a probability that the stimulus value s1 equals s2 and the result value r1 does not equal r2, said probability being computed from said probability that the stimulus value s1 equals s2 and said probability that the result value r1 equals r2.

12. The method of claim 7, wherein said sequential connection of said pair of memory elements includes an inversion between said pair of memory elements.

13. The method of claim 3, wherein said step of sequentially connecting memory elements includes sequentially connecting at least one pair of memory elements, said pair of memory elements being determined by a computing value extracted from the equation:

$$D(A,B) \{ 1 + K [pm(A)(1 - pm(B)) + pm(B) (1 - pm(A))] \}, \text{ wherein}$$

D(A,B) is a distance between said pair of memory elements,
pm(A) is a probability that said stimulus and result values of a first memory element of said pair are the same,
pm(B) is a probability that said stimulus and result values of a second memory element of said pair are the same, and
K is a constant value.

14. The method of claim 1, wherein test patterns are generated for said IC, at least one of said test patterns including a stimulus value which is undetermined for at least one of said memory elements, said undetermined stimulus value being set to a value which does not cause switching during a scan operation between said memory element and the nearest closest preceding memory element in said chain for which a value was determined by said test pattern.

15. The method of claim 1, wherein test patterns are generated for said IC, at least one of said test patterns including a stimulus value which is undetermined for at least one of said memory elements, said undetermined stimulus value being set to a value which does not cause switching during a scan operation between said memory element and the nearest closest following memory element in said chain for which a value was determined by said test pattern.

16. The method of claim 1, wherein test patterns are generated for said IC, at least one of said test patterns including a stimulus value which is undetermined for at least one of said memory elements and a result value which is determined for said at least one memory element, said undetermined stimulus value being set to coincide with said determined result value.

17. The method of claim 1, wherein test patterns are generated for said IC, at least one of said test patterns including a stimulus value which is determined for said at least one memory element, a result value which is undetermined for said at least one memory element, and stimulus values which are undetermined for at least another memory element, and wherein at least one of said undetermined stimulus values is set to a value which causes said undetermined result value to have a value that coincides to said determined stimulus value.

18. The method of claim 5, wherein said sequentially connecting said pair of memory elements is determined by computing a value determined by the equation:

$$D(A,B) \{ 1 + K [ps(1 - pr) + pr(1 - ps)] \}, \text{ wherein}$$

D(A,B) is a distance between said pair of memory elements,
ps is said probability that s1 equals s2,
pr is said probability that r1 equals r2, and
K is a constant value.

19. The method of claim 1, wherein a set of test patterns is generated for said IC, at least one pair of members of said test pattern set are merged to reduce the number of elements in said set of test patterns, a total switching activity during scan-in of said merged pattern is computed, and said merging is rejected if said computed total switching activity exceeds a predetermined limit.

20. The method of claim 1, wherein a set of test patterns is generated for said IC, a total switching activity during scan-out of result values for at least one member of said test pattern is computed, and said test pattern is rejected if said total computed switching activity exceeds a predetermined limit.

21. The method of claim 2, wherein a maximum switching activity during scan-in or scan-out of any test pattern of said set of test patterns is determined for at least one candidate scan chain ordering, said candidate scan chain ordering being rejected if said maximum switching activity exceeds said predetermined limit.

22. A method of reducing the switching activity during a test scan operation of at least one scan chain in an integrated circuit (IC) comprising the steps of:

a) generating a set of test patterns for said IC, comprising values that include at least one stimulus value for at least one memory element and at least one result value for another of said at least one memory elements;

b) determining from at least one of said test patterns at least one probability of coincidence between at least one pair of said values;

c) connecting said at least one memory element and said at least another memory element to form at least one scan chain based on said at least one probability; and

d) setting undetermined stimulus values in said test patterns to values that minimize switching activity during a scan operation based on the order of said memory elements connected in step c).

23. A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for reducing the switching activity during a test scan operation of at least one scan chain in an integrated circuit (IC), the method steps comprising:

a) determining stimulus and result value probabilities for a plurality of memory elements in said IC; and

b) connecting said memory elements to form at least one scan chain based on said probabilities, thereby reducing the switching activity as determined by the probabilities and by the ordering of said memory elements within said at least one scan chain.